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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,909	08/04/2003	Chen-Nan Yeh	67,200-1106	7571

7590 03/23/2005

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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,909	YEH ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-18 and 20-23* is/are rejected.

7)☒ Claim(s) *8,9 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-6 and 11-13 are rejected under 35 U. S. C. 102(e) as being anticipated by Ohuchi et al. (US 6,576,562, herein after Ohuchi).

Regarding claim 1, Ohuchi discloses in figs. 7A-4F a method for forming a dual damascene opening to protect a low-K dielectric insulating layer comprising the steps of: providing a semiconductor process wafer comprising a via opening extending though a thickness portion of at least one dielectric insulating layer 206 (fig. 7A); depositing a first dielectric layer 211 to seal the via opening (fig. 7C); blanket depositing a second dielectric layer stack 212 to form a hardmask over and contacting the first dielectric layer stack 211; photolithographically patterning and reactive ion etching through a thickness of the hardmask and the first dielectric layer stack to form a trench opening etching pattern overlying and encompassing the via opening while leaving the via opening sealed (fig. 7D; col. 27, line 63 through col. 28, line 8); and

reactive ion etching through a dielectric insulating layer to form a dual damascene opening (col. 28, lines 12-16 and lines 40-43).

Regarding claim 2, Ohuchi discloses that depositing the first dielectric layer stack 211forms a substantially planar upper surface (fig. 7C and col. 28, lines 32-33).

Regarding claim 3, Ohuchi discloses that removing the photoresist layer by an ashing process following the step of photolithographically patterning and etching (col. 28, lines 47-49 and col. 17, lines 15-17).

Regarding claims 4 and 5, Ohuchi discloses that dielectric insulating layer 206 comprises a low-K inter-metal dielectric (IMD) layer having a dielectric constant of less than about 3.9 (col. 23, lines 38-47).

Regarding claim 6, Ohuchi discloses that the dielectric insulating layer 206 consists essentially of the low-K IMD layer and an overlying dielectric anti-reflective coating (DARC) layer 207 selected from the group consisting of oxynitride, and oxycarbide (fig. 7B and col. 24, lines 11-54).

Regarding claims 11 and 12, Ohuchi disclose that the first and second dielectric layer stack 211/212 are selected from the group consisting of organic silicon oxide, oxycarbide, and hydrogenated oxycarbide (col. 26, line 63 through col. 27, line 31).

Regarding claim 13, Ohuchi discloses that carryout a subsequent reactive ion etching process to remove a remaining portion of the first and second dielectric layer stacks while removing a barrier layer 205 disposed at the via opening bottom portion to form closed communication with an underlying conductive area (figs. 7E-7F and col. 28, lines 49-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 7, 10, 14-18 and 20-23 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ohuchi (US 6,576,562) in view of Liu et al. (US Pat. 6,323,121, herein after Liu).

Regarding claims 7, 10, 14 and 18, Ohuchi discloses in figs. 7A-4F a method for forming a dual damascene opening to protect a low-K dielectric insulating layer comprising the steps of: providing a semiconductor process wafer comprising a via opening extending though a thickness portion of at least one dielectric insulating layer 206 (fig. 7A); depositing a first dielectric layer 211 to seal the via opening (fig. 7C); blanket depositing a second dielectric layer stack 212 to form a hardmask over and contacting the first dielectric layer stack 211; depositing a photoresist

layer 213 and photolithographically patterning (fig. 7C) and reactive ion etching through a thickness of the hardmask 212 and the first dielectric layer 211 stack to form a trench opening etching pattern overlying and encompassing the via opening while leaving the via opening sealed (fig. 7D; col. 27, line 63 through col. 28, line 8); carrying out a plasma ashing process to remove the photoresist layer without exposing an interior portion of the via opening (col. 28, lines 47-49 and col. 17, lines 15-17); and etching according to a second reactive ion etching process through a thickness portion of the dielectric insulating layer to form a dual damascene opening (col. 28, lines 12-16 and lines 40-43).

Ohuchi discloses the first and second dielectric layer 211/212 are formed by spin coating method and selected from the group consisting of organic silicon oxide, oxycarbide, and hydrogenated oxycarbide (col. 26, line 63 through col. 27, line 31). Ohuchi fails to disclose the first and second dielectric layer stacks are formed by CVD process. However, Liu teaches in col. 4, lines 15-25 that the organic polymer material is formed by PECVD. It would have been obvious to one with ordinary skill in the art at the time of the invention to form the first and second dielectric layer by PECVD process as taught by Liu in the process of Ohuchi. As recognized by one skilled in the art, the PECVD process is preferred because of the low deposition temperature (See Liu (col. 4, lines 24-25).

Regarding claims 15 and 16, Ohuchi discloses that dielectric insulating layer 206 comprises a low-K inter-metal dielectric (IMD) layer having a dielectric constant of less than about 3.9 (col. 23, lines 38-47).

Regarding claim 17, Ohuchi discloses that the dielectric insulating layer 206 consists essentially of the low-K IMD layer and an overlying dielectric anti-reflective coating (DARC)

layer 207 selected from the group consisting of oxynitride, and oxycarbide (fig. 7B and col. 24, lines 11-54).

Regarding claims 20 and 21, Ohuchi disclose that the first and second dielectric layer stack 211/212 are selected from the group consisting of organic silicon oxide, oxycarbide, and hydrogenated oxycarbide (col. 26, line 63 through col. 27, line 31).

Regarding claims 22 and 23, Ohuchi discloses that carryout a subsequent reactive ion etching process to remove a remaining portion of the first and second dielectric layer stacks while removing a barrier layer 205 disposed at the via opening bottom portion to form closed communication with an underlying copper conductive area; depositing and planarizing a copper layer 216 to fill the dual damascene opening (figs. 7E-7F and col. 28, lines 49-67).

Allowable Subject Matter

3. Claims 8, 9 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to

reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

March 19, 2005.